

Are FEDs coming back?

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Abstract

SED Inc., a joint venture of Toshiba and Canon, has announced to produce 55-inch Field Emission Displays (FEDs), which they call SEDs, in 2006. Besides this business information SED Inc. has also presented some technical details at two conferences in 2005. A review of this technical information in the context of some generic issues of FEDs will be presented.

Key words: field emission, flat panel display, luminescent efficiency, contrast, spacer, uniformity

Introduction

When SED Inc. exhibited 10 of their surface-conduction electron-emitter display (SED) panels at the big electronic and display show CEATEC Tokyo (Japan) in October 2005, crowds gathered and many people were impressed with the picture performance of the SED such as the high contrast, lack of motion artifacts, and wide color gamut. Since SED is a flat panel display (FPD) with a panel thickness of 7mm, many people wondered whether FEDs could compete with the dominant FPDs for large areas, notably LCDs and PDPs. So, the question is: are FEDs coming back in the display arena?

The recent history of FEDs is distressing. In recent decades, PixTech, Motorola, Candescent, Canon/Toshiba, Sony, Futaba, Samsung, and other companies spent substantially more than a billion dollars on the development of medium- and large-area FEDs. In spite of these efforts, Motorola stopped its industrialization of FEDs, while PixTech and Candescent went bankrupt. It's clear that the key issue with SED is not front-of-screen performance; it's scaling to mass production. Except for Futaba – which is ramping up a 3-inch FED for automotive applications now – this has been the downfall of every effort to date. But there are signs that this sad history may not repeat itself and that Phoenix arises from the ashes.

Although many FED soldiers were dropping around them, some groups pressed on with their R&D – especially on carbon nanotubes, which are considered to be more cost-effective field emitters than Spindt microtips. Last year, SED Inc., a joint venture of Canon and Toshiba, announced that 50-inch FEDs would be introduced to the market in 2006. The company has started pilot activities in Hiratsuka, Japan to support manufacturing. Samsung also announced production of large-format FEDs for TV by the end of 2006.

What makes FED so attractive that many companies continue to work on them when LCDs and PDPs are the dominant FPD technologies for TV? The main reason is that developers believe FEDs can be manufactured at lower cost than LCDs and PDPs. Furthermore, the picture performance is much like that of a CRT – which many people still considered the standard for TV – and the power consumption should be lower than that of PDPs and LCDs of the same size.

At Euro Display '96, Canon presented the principle of the Surface Conduction Electron Emitter (SCE) for FEDs [1]. This concept was revolutionary, since the paradigm for cold emission in FEDs at that time was an array of micro-tips. In 1999 Canon and Toshiba

started cooperation on the development of a surface-conduction electron-emitter display, and the publication of information on SCE-based FED development stopped.

The silence on SED was undone at the big CEATEC Japan 2004 electronics show, held near Tokyo in October 2004. Toshiba and Canon showed a 36-inch, wide-aspect-ratio SED. This year at CEATEC 2005, SED Inc. announced a midcourse correction, viz. that the forthcoming product would have a 55-inch diagonal, not 50 inches as originally stated.

Design of the SED

SED Inc. has presented in total three papers in 2005 on the design of a SED and its surface-conduction emitters, two at SID'05 in Boston in May 2005 [2, 3] and one at IDW/AD'05 in Takamatsu in December 2005 [4]. This information makes it possible to recognize some specific SED issues, and I will briefly review these in the context of some generic FED issues. Figure 1 shows a simplified cross section of a SED.

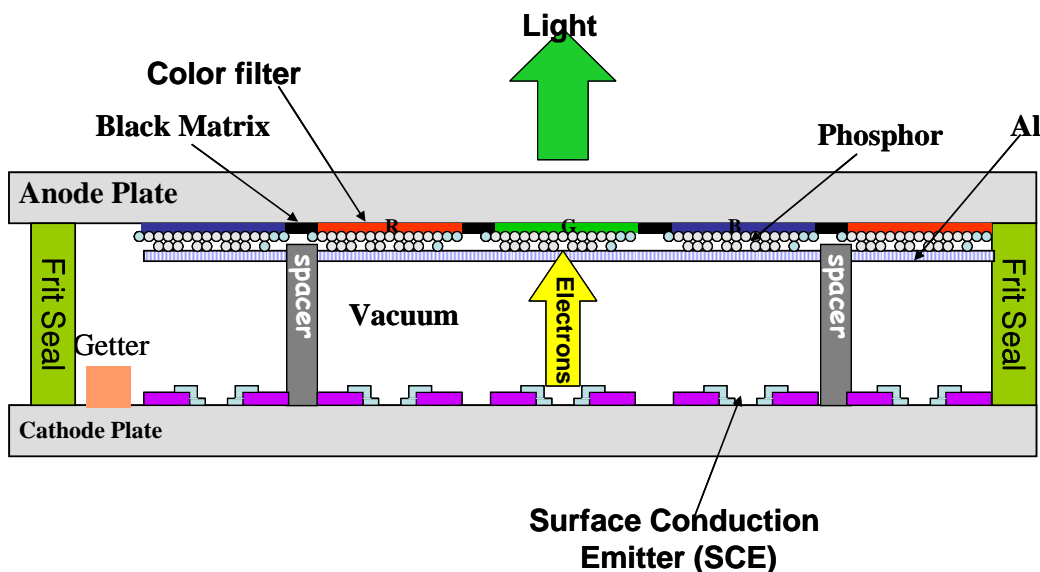


Figure 1. Cross section of SED. The anode plate of thin glass contains color filters, phosphor layers and Al-backing layer. Black matrix pattern is applied between the individual phosphor dots. The cathode plate contains the surface conduction electron emitters (SCEs), which are cold cathodes. Thickness of the panel is 7.3mm.

The luminous efficiency of a cathode luminescent display such as an FED is strongly dependent on the anode voltage: the higher the anode voltage the larger the luminous efficiency of the screen. In the 1990s a lot of R&D work was done on low-voltage phosphors for FEDs. Low-voltage phosphors are excited at low anode voltage, the advantage of which is high reliability. In the low-voltage application of FEDs electric breakdown (flash-over) at the spacers are rare: this explains the popularity of low-voltage FEDs in the R&D-community of the 1990s. But low-voltage phosphors have poor luminous efficiency, and using an aluminum backing layer – a trick that is used to increase the efficiency of high-voltage phosphors – doesn't work with low voltages. However, the largest hurdle in applying low-voltage phosphors is rather fast phosphor degradation during life because of the high current density. For that reason FEDs for TV need to apply anode voltages in the range of 7-12kV.

At 10 kV the luminous efficiency of an FED's screen could be as high as 15 lm/W. The SED has a screen efficiency of ~5lm/W for white light, because SEDs are equipped with contrast enhancing color filters, which reduce the light output. The second factor, which largely determines the luminous efficiency in FEDs, is the design of the contrast. The SED has been designed to get an extremely high contrast ratio in dark ambient light, viz. 10,000:1.

This is normally achieved with a rather thick Al-layer, which blocks the backscattered electrons from adjacent pixels. Backscattered electrons have a much lower energy than primary electrons and cannot pass the Al-layer. The power consumption of the 36-inch SED wide-format panel is 110 W (at 20 percent APL). This figure compares favorably to that of power-hungry PDPs and LCDs.

As mentioned above, the current density at the surface of the phosphor layer determines largely the lifetime of the phosphors: the larger the current density the shorter the life time. In the design of the SED this current density or phosphor loading is about 10 times larger than in a CRT, because of the rather small size of the electron spot and the application of a much smaller anode voltage: 10kV in stead of 30kV. In order to cope with this problem SED Inc. is applying a twin beam configuration: one phosphor dot is bombarded with two electron beams, as shown in figure 2. This configuration limits the beam spreading and controls the beam landing: an extra focusing grid is therefore not necessary. Since the two electron beams only partially overlap on the phosphor dot, the current density at the phosphor surface is minimized. Another advantage of this twin beam principle is a lower current density of the field emitters.

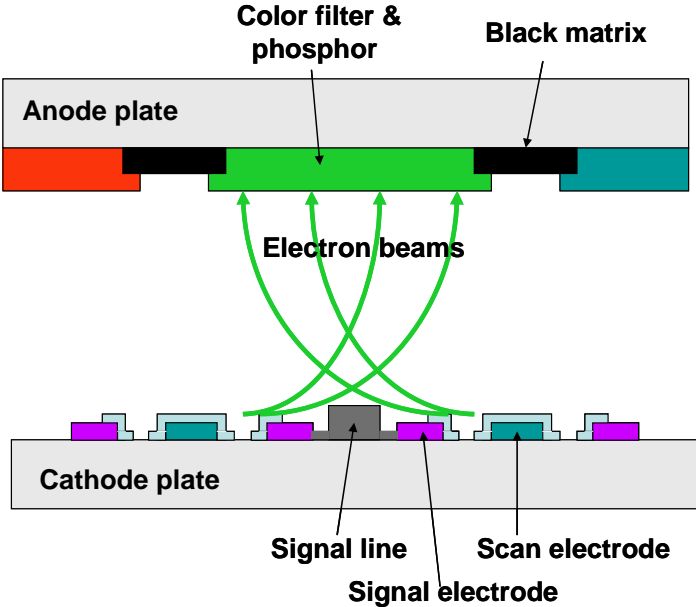


Figure 2. Twin beam principle. Two electron beams are landing on each phosphor. The electron spots on the phosphor do not overlap completely: in this way the phosphor loading is reduced. The electric field close to the emitters enables good focusing on the phosphor dot.

Besides the energy losses in the anode plate of SED needed to make light, the other power sink is in the cathode plate, since the efficiency of the surface conduction emitters is only 3 percent. This leads to rather high currents in the cathode plate with corresponding ohmic losses.

The contrast ratio of the SED at low ambient illumination is about 10,000, leaving LCDs far behind. The large black-matrix area and Toshiba’s color-filter technology yield a daylight contrast that is better than that of CRTs, which do not have color filters, but it is not as good as the daylight contrast of an LCD. Besides improving the daylight contrast, the color filters also widen the color gamut of the CRT-phosphors. In particular, the red color point becomes more saturated.

Spacers – strips or columns of glass that electrically insulate the cathode and anode plates while controlling the distance between these plates and counteracting the atmospheric pressure on the plates – can acquire a surface charge when hit by electrons, and are always an issue with FEDs from both the uniformity and reliability points of view. To suppress surface charging and high-voltage breakdown, spacers receive a coating or are made slightly conductive. In publications on FEDs, spacers are mostly treated in a step-motherly fashion – and this was the case in the SED papers presented in Boston and Takamatsu as well. In the SED samples shown at CEATEC 2005, the spacer strips with a height of 1.7mm were placed on the scan wires of the cathode plate and were virtually invisible. Figure 3 shows the position of one spacer and the matrix structure of the scan and signal wires. Two emitters at both sides of a signal wire form a twin as shown in figure 2.

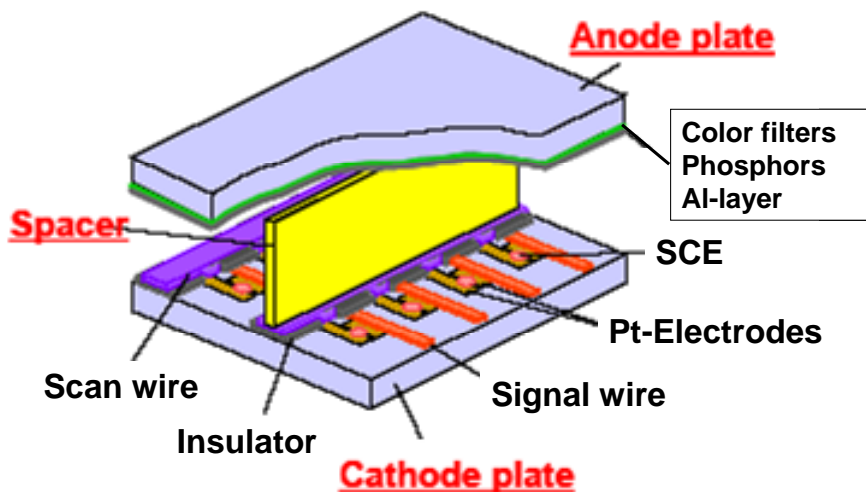


Figure 3. Perspective view of the SED. Spacer strip is positioned on top of a scan wire. Scan and signal wires form a matrix structure. Two adjacent SCEs at different sides of a signal wire form a twin

The uniformity of the emission from pixel to pixel is the hottest issue in FEDs besides spacer technology. The fairly good luminance uniformity of the SED implies that the tunneling currents of the individual pixels are identical within 2 percent. In the early publications on SCE it was stated that electron tunneling was achieved at small nano-gaps in a thin film of palladium oxide (PdO). Figure 4 shows the structure of the SCE with the PdO film and the nano-gap in detail.

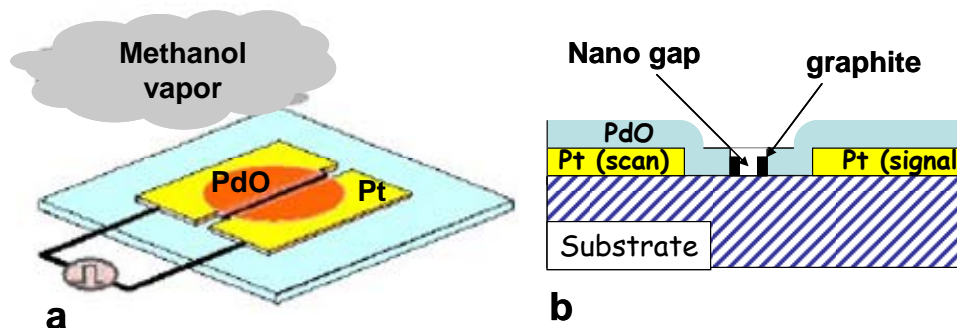


Figure 4. Surface Conduction Emitter. Formation of graphite (a) and structure of the nano-gap in the PdO-layer with graphite (b). Graphite is deposited in the gap by a CVD-process during electrical activation of the emitters.

Driving schemes for matrix displays such as PDPs, LCDs and FEDs are designed to improve luminance uniformity as well as to generate gray levels. The SED is a passive-matrix display using pulse-width modulation, but details weren't disclosed in the SID papers. At SID '05 we learned that it is essential to deposit graphite in the PdO nano-gap. The function of this graphite coating is still elusive; perhaps it is needed to control the gap width and to achieve in this way a uniform emission from pixel to pixel. The source of the carbon is an organic vapor such as acetone. The SCE current is reported as being very stable during (accelerated) life test. Lifetime of the luminance, i.e. the time for 50% decrease of the original luminance, of a SED, including the effect of phosphor degradation has not been published so far.

At this moment the peak luminance of an SED is limited to 400cd/m². It was said that the peak luminance could be increased to 500cd/m² in the near future. This is not as high as in CRTs, but the peak luminance is competitive with that in LCDs and PDPs for the time being.

Because of the fast-decaying P22 phosphors as used in CRTs, the response time for switching off is about 1ms, which enables excellent video performance without any motion artifacts.

Are FEDs really coming back?

Are FEDs coming back and should PDP-makers be afraid that this flat-panel Phoenix will arise from its own ashes? A FED such as the SED has much simpler drive electronics than a PDP, since it does not require energy recovery; compared with an LCD, the panel cost are much lower. However, the component prices alone do not determine the final cost. At this moment there is no information on the productivity of manufacturing SEDs. Motorola and Sony/Candescent were also able to show nice FED prototypes in the past, but they either failed to ramp up to volume manufacturing or decided not to start manufacturing at all. Recent history lead us to conclude that manufacturing of FEDs is difficult and that SED Inc. might need deep pockets to climb the learning curve for manufacturing.

Another question is how will SED Inc. position its 55-inch SED – the company's first intended product – in the market? FEDs could be a low-power alternative for PDPs and large-format LC-TVs. Another option is to focus on the excellent contrast and video performance without motion artifacts such as blurring and false contouring.

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Brief Biography



Daniel den Engelsen (1941) got his Ph.D (Chemistry) in 1968 at the University of Utrecht (The Netherlands). He worked in Philips Research and Philips Display Components from 1968-2004. He retired in 2004. Experience: CRT-technologies, FED-technologies, light and electron optics, phosphor technology, spectroscopy and solid-state chemistry.

In 2002 he was awarded as Fellow of the SID.

Now he is visiting professor at Southeast University in Nanjing and the University of Electronic Science and Technology of China in Chengdu.

Present areas of research and interest: cathodes, luminescence, FEDs, backlights for LCDs and gas discharge phenomena.