PolyApply The Application of Polymer Electronics to Ambient Intelligence

Organic Electronics:
a disruptive technology

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The technical approach to technology roadmapping: a management view

Bill Eccleston

'the cornerstone of strong product management
is the technological competence of the manager'

Gordon Moore 1975 (Intel)

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'PolyApply'

(started January 2004)

Board Members: ST, Philips, Motorola,Merck-Avecia, Plastic Logic, IMEC, Fraunhofers, LETI, Liverpool University

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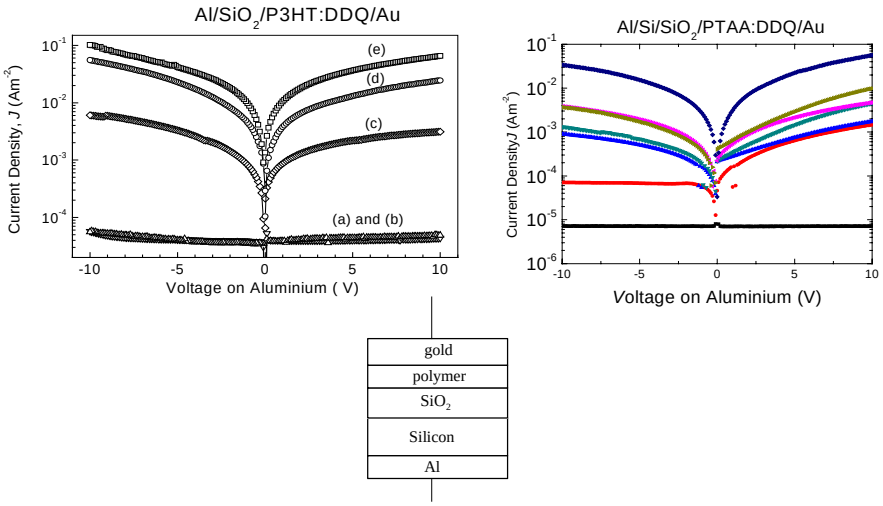
- MOS & Bipolar Projects Manager: Caswell
- Technical Consultant: Displays Division GEC (Wembley)
- Chairman: Rytrak Ltd (Equipment for Displays industry)
- Technical Director: UK Light Thin Displays (wholly owned by Akhter Computer Holdings)
- 25 Licensed Patents, 6 in Organics.
- Rankin Professor/ Royal Academician: Liverpool University: (group of 16 people)

Warning



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Current status of organic electronics:

- materials have greatly improved in the last three years.
- much improvement still needed.
- manufacturing techniques yet to be agreed, but some advanced form of printing will win.
- currently no scaling rules to give optimum dimensions for roadmaps
- manufacturers of reel to reel print machines are key players: scaling (& hence roadmapping) is also for them
- rf tags represent the front-runner and it will be disruptive to item barcode
- air sensitive: packaging problems still have to be resolved
- displays will benefit from very large market for disposable tags.
- low cost organic displays on flexible will be disruptive to other forms of AMCLD
- much depends on the cost of organic materials when produced in bulk.

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Who benefits from roadmapping at such an early stage:

- product managers
- production equipment developers
- Investors
- potential users
- Competitors
- trainers

Consequence of weak/wrong roadmapping

- misdirected development work
- wasted investment funds
- project drag through poor focus
- extension of life of old methods
- unwanted trained people

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'rf tags represent the front-runner and it will be disruptive to item barcode'

Why?

Because Wal-mart will insist that almost all the items that it sells have individual rf tags and item suppliers will pay

Why?

Because that is what they are doing with silicon rf tags for 'slap and ship' Deadline January 2006

Why?

Because they have severe logistical problems.

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2004 Baltimore conference of EPC on rf id market: business led by Wal-mart, need to interrogate items within cartons, printable organic tags needed soon. Retail and health sectors leading with military also ahead.

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Technical Roadmapping of rf tags(transistors and diodes)*

- from conduction models develop device physics.
- from device physics determine scaling factors.
- with known performance requirements** scale the device parameters.
- from scaling requirements develop specification of equipment requirements.
- have a standard process which is flexible with respect to the polymer, surface treatments, introduction of a variety organic materials for conductors and diodes. Will provide all the data for implementation of technical roadmap.
- also developing circuit roadmapping

** performance requirements come from business roadmap

* In collaboration with adria

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Scaling Rules: management tool in c-Si

If we multiply channel length by 1/S,

we must multiply dopant density by S,

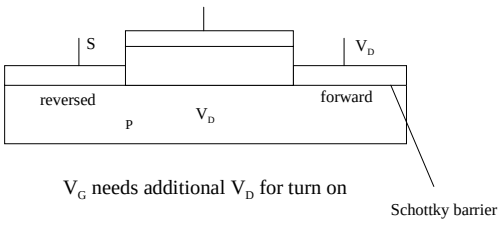
we must reduce increased V_T by multiplying gate dielectric thickness by 1/S,

but pressure to reduce V_{DD} so make dielectric scaling $1/S^2$ or introduce hi-K dielectrics

circuit speed $\propto 1/L^2$ so it scales with $1/S^2$

etc for other parameters: hence Moore's Law.

Non ideal source and drain



This will limit performance: needs to included in scaling rules and models.

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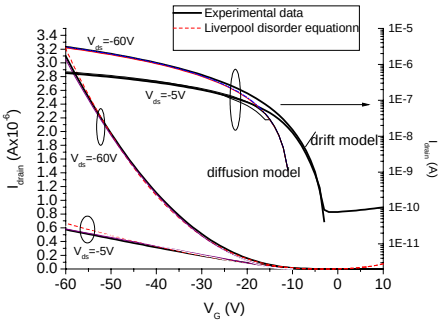
Device Models in conjunction with CEA LETI (and Silvaco)

disordered material:

$$I = \frac{W}{L}\frac{K}{C(C+1)}\frac{C_o^{\,C}}{\left(2\varepsilon_o\varepsilon_p kT\right)^m}\left[\left(V_{G'}-V_D\right)^{C+1}-V_{G'}{}^{C+1}\right]$$



polycrystalline material:

$$I = \left(\frac{W}{L}\right)\left(\frac{2A}{C(C+1)D^C}\right)\left[\left(V_{G'}-V_D\right)^{C+1}-V_{G'}{}^{C+1}\right]$$

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Scaling Rules: management tool in Organics

- to increase yield and reliability we multiply channel length by 1/S,
- to overcome imperfect contacts must multiply residual stable dopant density by S,
- to reduce off current multiply polymer film thickness by 1/S
- to reduce power reduce V_T by multiplying gate dielectric thickness by 1/S,
- circuit speed $\propto 1/L^2$ so it scales with $1/S^2$

etc for other parameters: hence Moore's Law.

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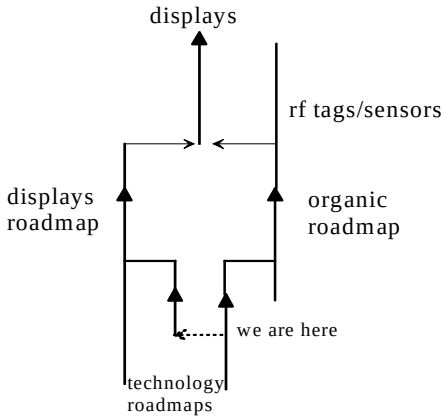

ADRIA Meeting:Amsterdam

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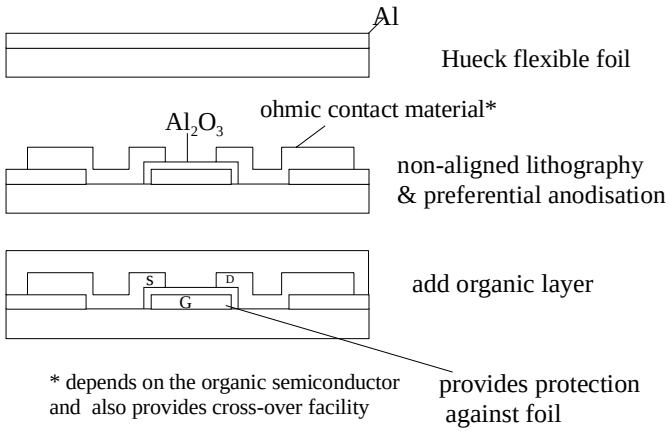
Conclusions

- organic stability problems are serious
- yield problems are likely to also be critical
- they are different from those experienced with silicon
- good simulation models continue to be produced
- they lead to simple scaling rules for use by management
- they inform, when coupled with a roadmap, a wide range of peripheral suppliers
- we cannot easily fix time scales but take-off will be very rapid and will be disruptive to barcode
- the existence of a strong and growing market in tags will lead to an attempt to disrupt other compatible products (ie displays)
- our main task is to produce a framework for the ongoing development of successive roadmaps

ADRIA: Amsterdam meeting, February 2005

Ideal Process



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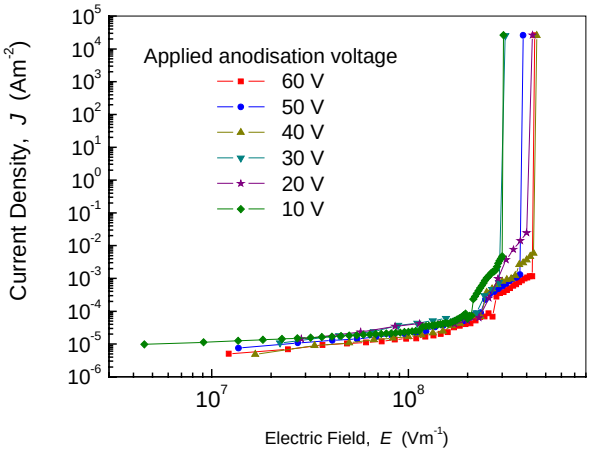
Yield determining factor: gate dielectric?

Recent Result:



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Calculation of diode or TFT capacitance

Exponential distribution used as approximation to Gaussian distribution of states using an effective temperature T_D gives effective Debye Length L_D:

$$L_D = \left[\frac{\varepsilon_0 \varepsilon_p k T_D}{q^2 n}\right]^{1/2} \quad where \left(\frac{1}{T_D}\right) = \left(\frac{1}{T}\right) - \left(\frac{2}{T_C}\right)$$

•Accumulation layer n=$n_{surface}$ capacitance= $\varepsilon_p\varepsilon_0/L_D$; oxide capacitance $\varepsilon_0\varepsilon_d/x_t$

•Drift dominates when V_{DS} >10kT_D since:

$$J_{diff} = qD\left(\frac{dn}{dx}\right) = qD\left(\frac{n(0)}{L}\right) = q\mu n(0)\left[\frac{kT_D/q}{L}\right]$$

•Abrupt depletion edge approximation applies when classic depletion layer thickness greater than L_D and n in equation for L_D is equal to doping concentration.

• attempting soon to find T_D by measurement of T_C as a function of temperature T for all organics in PolyApply.

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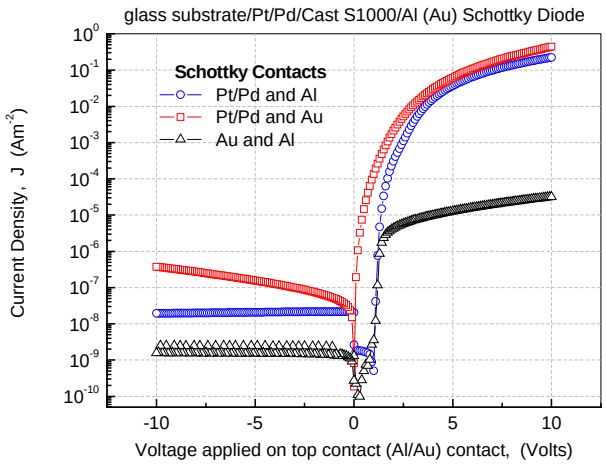
Diode fabrication and device physics



What next?

- continue training and dissemination work
- accelerate scaling activities.
- develop business roadmap.
- develop ideal ‘whole-process’
- produce text-book and give trial course to undergraduates
- more work on ‘ionic’ stability
- complete device models and implement in Silvaco software: for novel circuit development
- produce CCD: currently at mask stage.
- produce dual dielectric memory transistor and find how to use it.
- innovative circuit design.
- plan ICOE 2006

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